WHAT IS CLAIMED IS:

1. A voltage level shift circuit comprising:

a power detection circuit which generates a control signal in response to a first power supply voltage and a second power supply voltage;

an input circuit, connected between the first power supply voltage and a ground voltage, which receives an input signal and outputs a signal; and

an output circuit, connected between the second power supply voltage and the ground voltage, which generates an output signal in response to the control signal and the signal output from the input part.

2. The circuit according to claim 1, wherein the power detector comprises:

a first voltage divider, connected between the first power supply voltage and the ground voltage, which outputs a signal according to a voltage level of the first power supply voltage;

a second voltage divider, connected between the second power supply voltage and the ground voltage, which divides the second power supply voltage in response to the signal output from the first voltage divider;

a comparator which compares the signal output from the first voltage divider with an output of the second voltage divider; and

an inverter which receives an output of the comparator and which outputs the control signal.

3. The circuit according to claim 2, wherein the first voltage divider comprises:

a PMOS transistor having a source connected to the first power supply voltage, a drain and a gate;

a first resistor having one end connected to the ground voltage and

the other end connected to the drain of the PMOS transistor as an output of the first voltage divider; and

a second resistor having one end connected to the ground voltage and the other end connected to the gate of the PMOS transistor.

4. The circuit according to claim 2, wherein the second voltage divider comprises:

a first PMOS transistor having a source connected to the second power supply voltage, a drain and a gate, the drain and the gate of the first PMOS transistor being connected to each other;

a second PMOS transistor having a source connected to the drain of the first PMOS transistor, a drain and a gate, the drain and the gate of the second PMOS transistor being connected to each other;

a third PMOS transistor having a source connected to the drain of the second PMOS transistor, a gate connected to receive the signal output from the first voltage divider, and a drain; and

an NMOS transistor having a drain connected to the drain of the third PMOS transistor, a source connected to the ground voltage and a gate connected to receive the output of the first voltage divider.

5. The circuit according to claim 2, wherein the comparator comprises:

a first PMOS transistor having a source connected to the second power supply voltage, a drain and a gate;

a second PMOS transistor having a source connected to the second power supply voltage, a drain and a gate;

a first NMOS transistor having a drain connected to the drain of the first PMOS transistor and the gate of the second PMOS transistor, a gate connected to receive the signal output from the first voltage divider, and a

source connected to the ground voltage; and

a second NMOS transistor having a drain connected to the drain of the second PMOS transistor and the gate of the first PMOS transistor, a gate connected to receive the output of the second voltage divider, and a source connected to the ground voltage.

6. The circuit according to claim 1, wherein the input part comprises:

a first inverter which receives the input signal; and

a second inverter which receives an output of the first inverter.

7. The circuit according to claim 6, wherein the input part outputs a first signal from the first inverter and a second signal from the second inverter, and wherein the output part comprises:

a first PMOS transistor having a source connected to the second power supply voltage, a gate connected to receive the control signal, and a drain;

a second PMOS transistor having a source connected to the second power supply voltage, a gate connected to receive the control signal, and a drain;

a third PMOS transistor having a source connected to the drain of the first PMOS transistor, a drain and a gate;

a fourth PMOS transistor having a source connected to the drain of the second PMOS transistor, a drain and a gate;

a first NMOS transistor having a drain connected to the drain of the third PMOS transistor and the gate of the fourth PMOS transistor, a gate connected to receive the first signal output from the input part, and a source connected to the ground voltage;

a second NMOS transistor having a drain connected to the drain of

the fourth PMOS transistor and the gate of the third PMOS transistor, a gate connected to receive the second signal output from the input part, and a source connected to the ground voltage;

a third NMOS transistor having a drain connected to the drain of the first NMOS transistor, a source connected to the ground voltage and a gate connected to receive the control signal; and

an inverter having an input connected to the drains of the first and third NMOS transistors and an output connected to output the output signal.

8. A power detecting circuit comprising:

a first voltage divider, connected between a first power supply voltage and a ground voltage, which outputs a signal according to a level of the first power supply voltage;

a second voltage divider, connected between the second power supply voltage and the ground voltage, which divides the second power supply voltage in response to the signal output from the first voltage divider;

a comparator which compares the signal output from the first voltage divider with an output of the second voltage divider; and

an inverter which receives an output of the comparator and which outputs a control signal indicative of whether at least one of the first and second power supply voltages is interrupted.

9. The circuit according to claim 8, wherein the first voltage divider comprises:

a PMOS transistor having a source connected to the first power supply voltage, a drain and a gate;

a first resistor having one end connected to the ground voltage and the other end connected to the drain of the PMOS transistor as an output of the first voltage divider; and

a second resistor having one end connected to the ground voltage and the other end connected to the gate of the PMOS transistor.

10. The circuit according to claim 8, wherein the second voltage divider comprises:

a first PMOS transistor having a source connected to the second power supply voltage, a drain and a gate, the drain and the gate of the first PMOS transistor being connected to each other;

a second PMOS transistor having a source connected to the drain of the first PMOS transistor, a drain and a gate, the drain and the gate of the second PMOS transistor being connected to each other;

a third PMOS transistor having a source connected to the drain of the second PMOS transistor, a gate connected to receive the signal output from the first voltage divider, and a drain; and

an NMOS transistor having a drain connected to the drain of the third PMOS transistor, a source connected to the ground voltage and a gate connected to receive the output of the first voltage divider.

11. The circuit according to claim 8, wherein the comparator comprises:

a first PMOS transistor having a source connected to the second power supply voltage, a drain and a gate;

a second PMOS transistor having a source connected to the second power supply voltage, a drain and a gate;

a first NMOS transistor having a drain connected to the drain of the first PMOS transistor and the gate of the second PMOS transistor, a gate connected to receive the signal output from the first voltage divider, and a source connected to the ground voltage; and

a second NMOS transistor having a drain connected to the drain of

the second PMOS transistor and the gate of the first PMOS transistor, a gate connected to receive the output of the second voltage divider, and a source connected to the ground voltage.

12. A voltage level shift circuit comprising:

a first power supply node which supplies a first voltage level during a normal operational mode;

a second power supply node which supplies a second voltage level during the normal operational mode;

an input circuit which is connected to the first power supply node and which receives an input signal and generates a corresponding output signal having the first voltage level during the normal operational mode;

an output circuit which is connected to the second power supply node and which receives the signal having the first voltage level and which generates a corresponding output signal having the second voltage level during the normal operational mode; and

a detection circuit which detects an interruption in the supply of the first voltage level by the first power supply node, and which electrically blocks at least one leakage current path in the output circuit during the interruption.

13. The circuit according to claim 12, wherein the interruption occurs during a power-down operational mode.

14. The circuit according to claim 12, wherein the output circuit comprises an inverter having an input that is grounded in response to the interruption detected by the detection circuit.